A 2-GHz RF Front-End Transceiver Chipset in CMOS Technology for PCS and IMT-2000 Applications

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Abstract — **This paper describes RF front-end transceiver chipset for the dual-mode operation of PCS and IMT-2000. The transceiver chipset has been implemented in a 0.25μm single-poly five-metal CMOS technology. The receiver IC consists of a LNA and a down-mixer, and the transmitter IC integrates an up-mixer. Measurements show that the transceiver chipset covers the wide RF range from 1.8GHz for PCS to 2.1GHz for IMT-2000. The LNA has 2.5~2.8dB NF, 13~12dB gain and 6~4dBm IIP3. The down mixer has 15.5~16.0dB DSB NF, 15~13dB power conversion gain and 2~0dBm IIP3. The up mixer has 0~-2dB power conversion gain and 6~3dBm OIP3. With a single 3.0V power supply, the LNA, down-mixer, and up-mixer consume 5mA, 30mA, and 25mA, respectively.**

I. Introduction

The progress of wireless communication services has increased the need for communication systems which have low cost, low power, and multiband capabilities. It is desirable to combine two or more standards in one mobile unit for overall capacity enlargement, higher flexibility, and roaming capability as well as backward compatibility. Moreover, multi-standard transceivers will allow access to different systems providing various services. These are the cause of the instigation for the multi-band multi-mode operation.

This paper presents the design and implementation of a pair of dual-band CMOS RF front-end transceiver ICs for PCS and IMT-2000 standards. Section II describes the design of the building blocks. Experimental results are presented in Section III and the paper is summarized in Section IV.

II. RF Transceiver Design

This prototype CMOS RF front-end transceiver chipset is intended for PCS (Korea) and IMT-2000 mobile units. The simplified block diagram of the RF front-end transceiver is shown in Fig. 1. The receiver IC consists of an LNA, a down-conversion mixer, and the transmitter IC integrates only an up-conversion mixer. The designed transceiver ICs together with external band-select filters and a power amplifier including driver, complete the RF front-end and interface with the IF signal block providing channel selection filter, variable gain amplifier, IF-BF conversion mixer, and low pass filter.

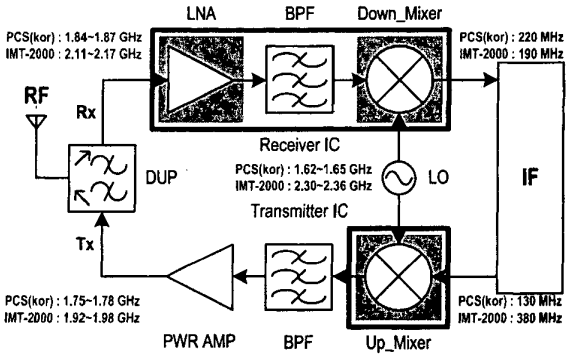

Fig. 1. Simplified RF front-end transceiver architecture.

A. Low Noise Amplifier (LNA)

The primary goal of a LNA is to keep the overall noise figure of the receiver low enough by screening the relatively large noise of the following mixer by the gain of the LNA. The essential requirements of a LNA are low noise, high gain, high linearity, and low power consumption.

The inductively degenerated LNA depicted in Fig. 2 is the most suitable from the above requirements standpoint as well as input 50Ω matching [1]. It is well known that the resistive part in the input impedance can be expressed as (gm/Cgs)*Ls of the input stage. The cascode transistor (M2) provides better reverse isolation and alleviates the miller effect of the Cgd of M1.

The LNA biasing current and transistor size must be chosen to optimize the above requirements. The M1 was decided to drain 5mA biasing current and to have 200μm total gate width. The width of M2 was selected to 100μm by considering the gain and output 50Ω matching. To reduce the noise occurred by gate resistance, all the transistors have multi-fingered structure with unit 5μm gate width and have meander type double-sided gate

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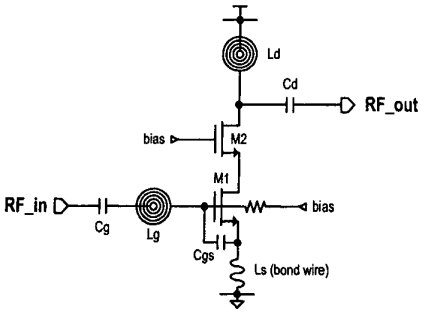


Fig. 2. LNA schematic.

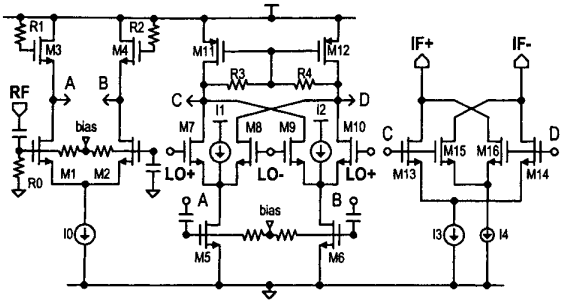


Fig. 3. Down-mixer schematic.

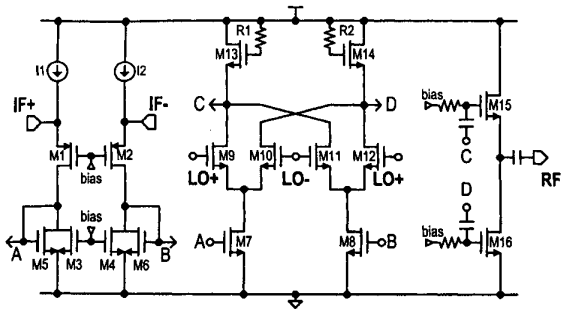


Fig. 4. Up-mixer schematic.

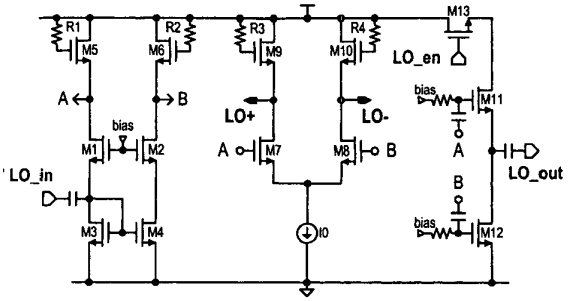


Fig. 5. LO balun and LO buffer schematic.

contact [2]. The circular spiral inductors (Lg and Ld) have 7nH and 6nH, respectively. The bond wire inductor (Ls) has about 1nH. Noise consideration requires that the Lg should be a low loss inductor. The measured quality factor of the spiral inductors is above 8 at 2GHz with the help of 2μm-thickness top metal. Thus, the Lg as well as Ld are integrated on the chip for low cost and high integration. The Ld and Cd form the L-matching network for optimal power transfer to the following stage. The Cd as well as Cg is utilized as dc blocking capacitors excluding low frequency harmonic components.

B. Down Mixer

The LNA output signal is filtered by LC band pass filter and down converted to IF frequency by the down mixer shown in Fig. 3. The down mixer must have sufficient conversion gain with a minimal noise contribution. Therefore, the down mixer was realized with an active mixer resembling the bipolar Gilbert cell analog multiplier. The down mixer has three-stage configuration composed of a single to differential amplifying balun, a double balanced Gilbert cell mixer, and an output driver.

The R0 is used for input 50Ω matching. It is possible to use higher resistance than the required resistance for matching. This is due to the fact that the R0 can be shown in lower resistance when parasitic bond & package inductance and parasitic pad & gate capacitance are series resonance. By using higher resistance over 100Ω than 50Ω resistance, we minimize the noise contribution as small as possible.

The single-ended input signal is transformed to differential signal for driving double balanced mixer input transistors, and amplified for improving noise figure degradation. The transistors (M3, M4) so called active inductor load are employed to increase and flatten the gain in the desired RF band. Since, the transistors (M5, M6) have large bias current to increase the linearity, we choose current bleeding (I1, I2) method to reduce the LO overdrive required for complete switching and thus effectively to increase the conversion gain.

The mixer output driver is composed of four transistors (M13~M15) and two current source (I3, I4). To remove the third-order intermodulated signal components, we adopted the linearization technique of adding the cross coupled structure (M15, M16) to the typical differential pair (M13, M14). The driver has open-drain output nodes to adapt various impedance matching such as 1KΩ for PCS and 200Ω for IMT-2000.

C. Up Mixer

To perform the frequency translation from IF to RF, the modified double-balanced Gilbert quad active mixer is

used in the up-conversion mixer as shown in Fig. 4. The up mixer has three-stage configuration composed of a common gate differential amplifier, a double balanced mixer and an output driving buffer.

The common gate transistors (M1, M2) have a wide band constant resistance suitable to input impedance matching for 130MHz PCS and 380MHz IMT-2000. Since the mirrored gain is proportional to the ratio of the driving transistors (M5, M6) and the driven transistors (M7, M8), the latter must be larger than the former in order to achieve the desired gain. However, the biasing currents of the M7 and M8 are also increased as much as the mirrored gain. So the transistors (M3, M4) are employed to adjust the bias current of the M7 and M8. The output driving buffer has the push-pull structure combined with a common-source transistor (M16) to boost the signal and a source follower transistor (M15) to drive the external matched 50Ω impedance.

D. LO Balun and LO Buffer

The LO processing block is composed of a LO balun and a LO buffer as shown in Fig. 5. The LO balun transforms the single-ended LO input signal to differential signal for driving the LO quad transistors in the down and up mixer. The bisymmetric Class-AB topology (M1~M4) based on translinear principles was selected to the LO balun. Compared with typical differential pair converters, this topology can enable us to get the wide band 50Ω resistance suitable to impedance matching from 1.62GHz PCS to 2.36GHz IMT-2000. In the down mixer of the receiver IC, the LO buffer is required to enable other circuits to be switched on or off depending on the status of the transceiver modes. We design the LO buffer using a switching transistor (M13) and the push-pull structure (M11, M12) mentioned above.

III. Experimental Results

The RF front-end transceiver chipset has been designed with the RF device models and fabricated in a standard 0.25μm single-poly, five-metal CMOS technology. Fig. 6 shows the die photos of the receiver and transmitter ICs. Their die areas including the bonding pads are 2.4x1.4 mm^2 and 1.4x1.2 mm^2, respectively. All transistors passing through differential signal have a common centroid layout to improve balancing. The LNA and mixer of the receiver have been laid out as stand-alone circuits and were tested and characterized individually Fig. 7 shows the printed circuit board for testing the receiver and transmitter ICs, which were packaged using SSOP-24pin and SOIC-8pin package, respectively. We use double or triple bonds to minimize the bond wire inductance. As shown in Fig. 7, only a few support components are used

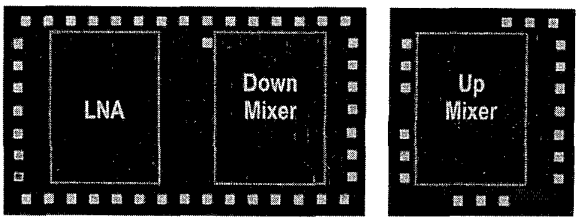


Fig. 6. Micrograph of the RF front-end transceiver chips.

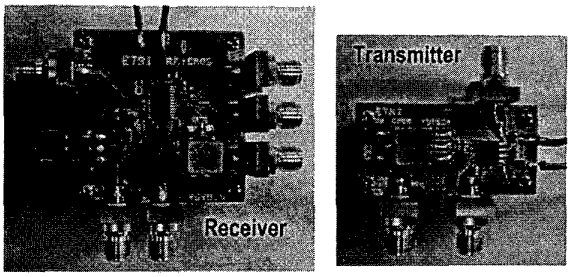
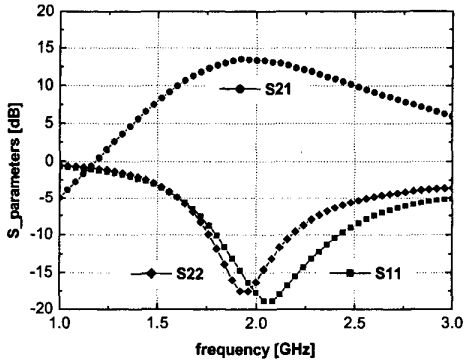


Fig. 7. Transceiver ICs mounted on printed circuit boards.



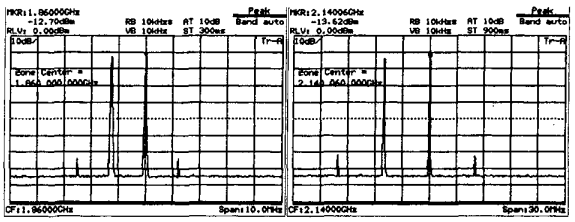


Fig. 8. Measured results of the LNA.
(RF= -25dBm at 1.86GHz & 2.14GHz)

with the exception of the IF balun transformers for impedance transformation from IF matching impedance to measurement 50Ω setup.

With a single 3.0V power supply, the LNA, the down-mixer, and the up-mixer consume 5mA, 30mA, and 25mA,

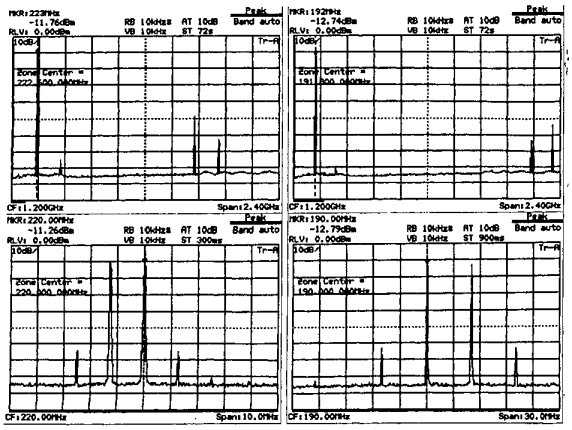


Fig. 9. Frequency spectrum of the down-mixer.
(RF= -25dBm at 1.86GHz & 2.14GHz, LO= -5dBm at 1.64GHz & 2.33GHz)

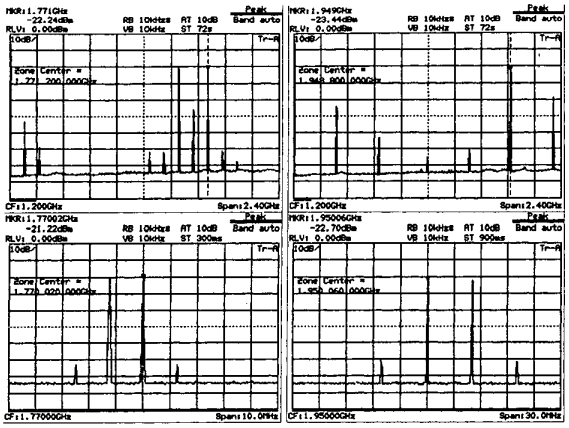


Fig. 10. Frequency spectrum of the up-mixer.
(IF= -20dBm at 130MHz & 380MHz, LO= -5dBm at 1.64GHz & 2.33GHz)

respectively. The measured results of the LNA are shown in Fig. 8. Around 2GHz, the LNA has 2.5~2.8dB NF, 13~12dB gain, 6~4dBm IIP3 and less than -12dB return loss. Fig. 9 and Fig. 10 show the measured frequency spectrum of the down and up mixer. The overall power loss in down and up mixer measurement setup is assumed as about 2dBm. This value is very reasonable considering the losses of balun transformers and cables. The measurements show that the down mixer has 15.5~16.0dB double side band (DSB) NF, 15~13dB power conversion gain, 2~0dBm IIP3 and less than -10dB return loss. The NF of the down mixer is a little high because of using the rigid resistor (R0) for input impedance matching as shown in Fig. 3. And the up mixer has 0~-2dB power conversion gain, 6~3dBm OIP3 and less than -15dB return loss.

TABLE 1
TRANSCEIVER PERFORMANCE SUMMARY

Technology / Supply Voltage	0.25um CMOS 1P5M, 3.0 V		
	PCS	**IMT-2000**	Unit
Receiver IC (LNA + Down Mixer : Idc = 35mA)			
LNA (Idc = 5mA)			
Gain	13	12	dB
Input IP3	+6	+4	dBm
Noise Figure	2.5	2.8	dB
In/Out return loss	-12 / -15	-18 / -12	dB
Reverse Isolation	30	30	dB
Down Mixer (Idc = 30mA)			
Conversion Gain	15	13	dB
Input IP3	+2	0	dBm
Noise Figure (DSB)	15.5	16.0	dB
RF/LO return loss	-12 / -16	-10 / -18	dB
LO to RF/IF Isolation	35 / 30	30 / 30	dB
Transmitter IC (Up Mixer : Idc = 25mA)			
Conversion Gain	0	-2	dB
Output IP3	+6	+3	dBm
RF/LO return loss	-15 / -17	-16 / -20	dB
LO to RF/IF Isolation	30 / 35	25 / 35	dB
LO Leakage	-40	-35	dBm

IV. CONCLUSION

We present the design and implementation of dual-band CMOS RF front-end transceiver ICs for PCS (Korea) and IMT-2000 standards. Since the presented transceiver shares its building blocks in both the standards, it is as simple and small as possible. The transceiver has been implemented in a standard 0.25μm CMOS technology. The receiver IC consists of a LNA and a down-mixer, and the transmitter IC integrates an up-mixer. With a single 3.0V power supply, the LNA, down-mixer and up-mixer consume 6mA, 30mA and 25mA, respectively. The overall measured performances are summarized in table 1.

ACKNOWLEDGEMENT

The authors wish to acknowledge the assistance and support of the *Hynix* Semiconductor Inc.

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